

Fig. 1

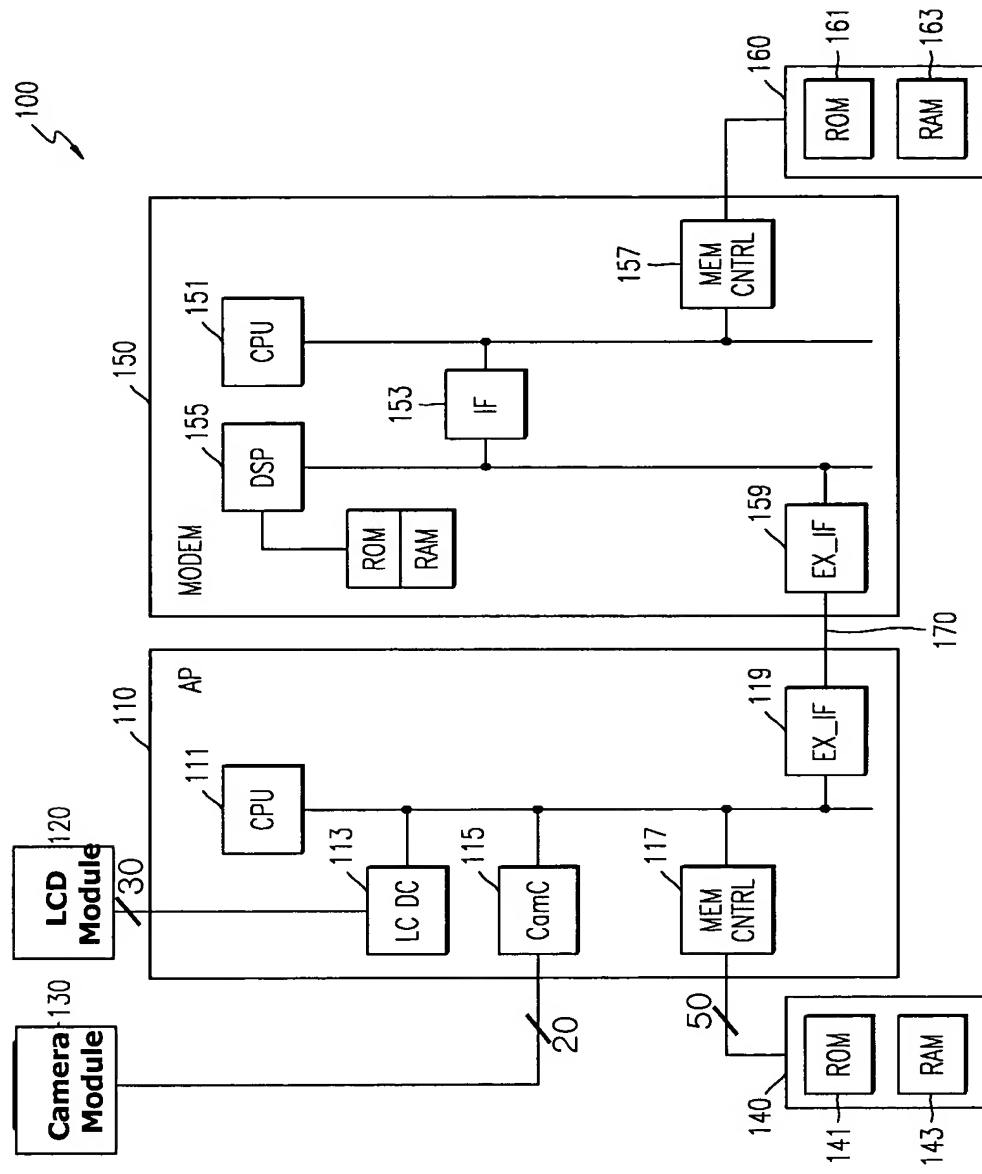


Fig. 2

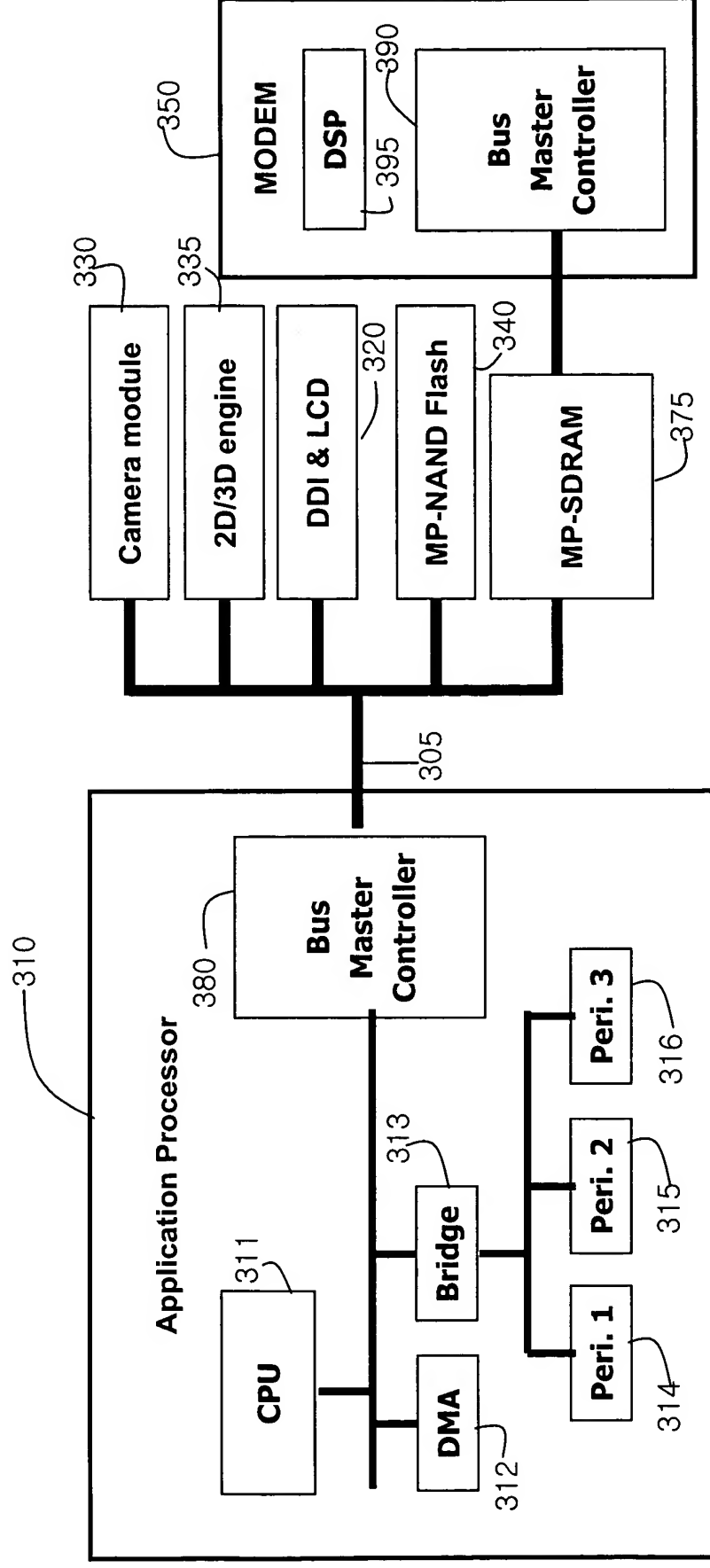


Fig. 3

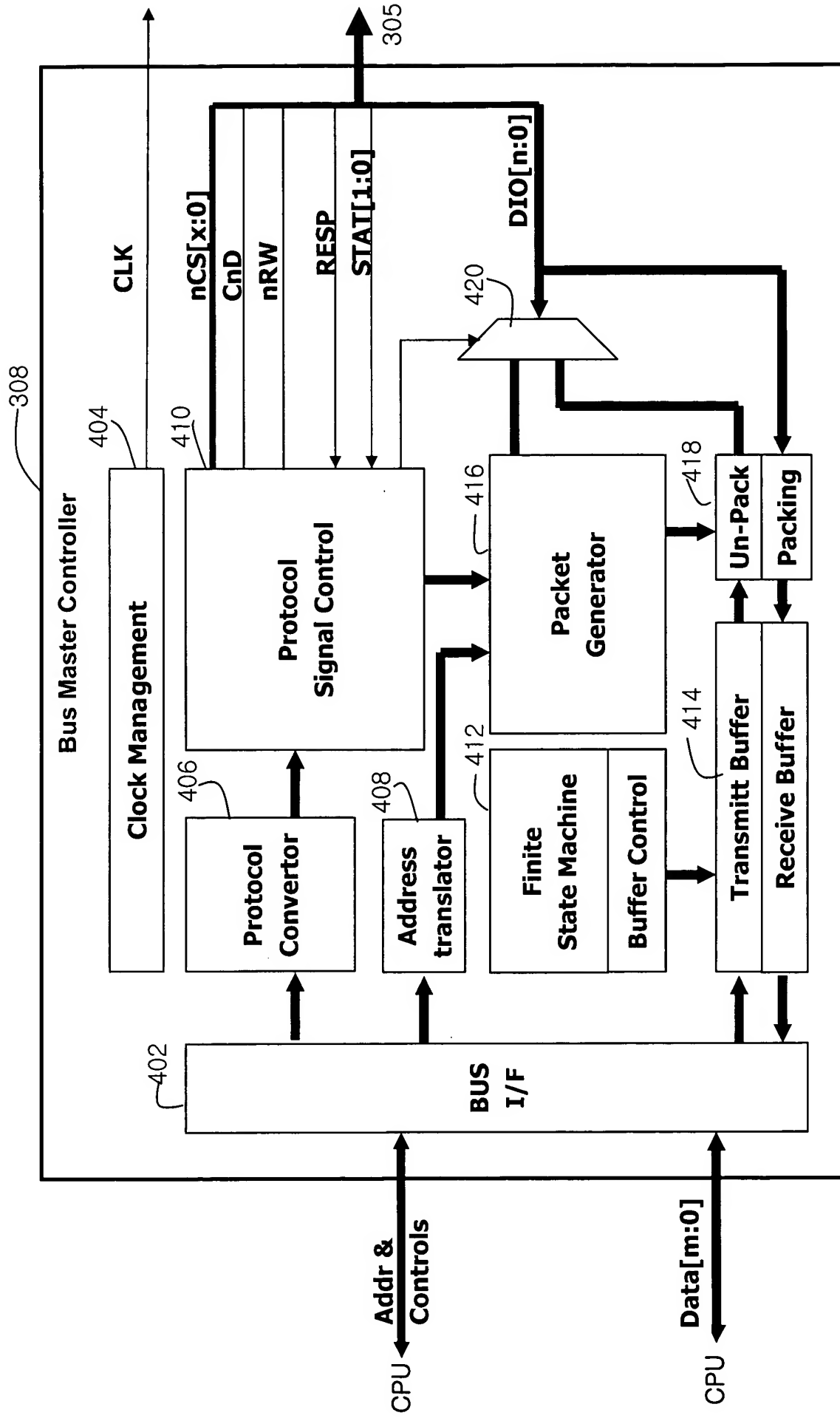


Fig.4

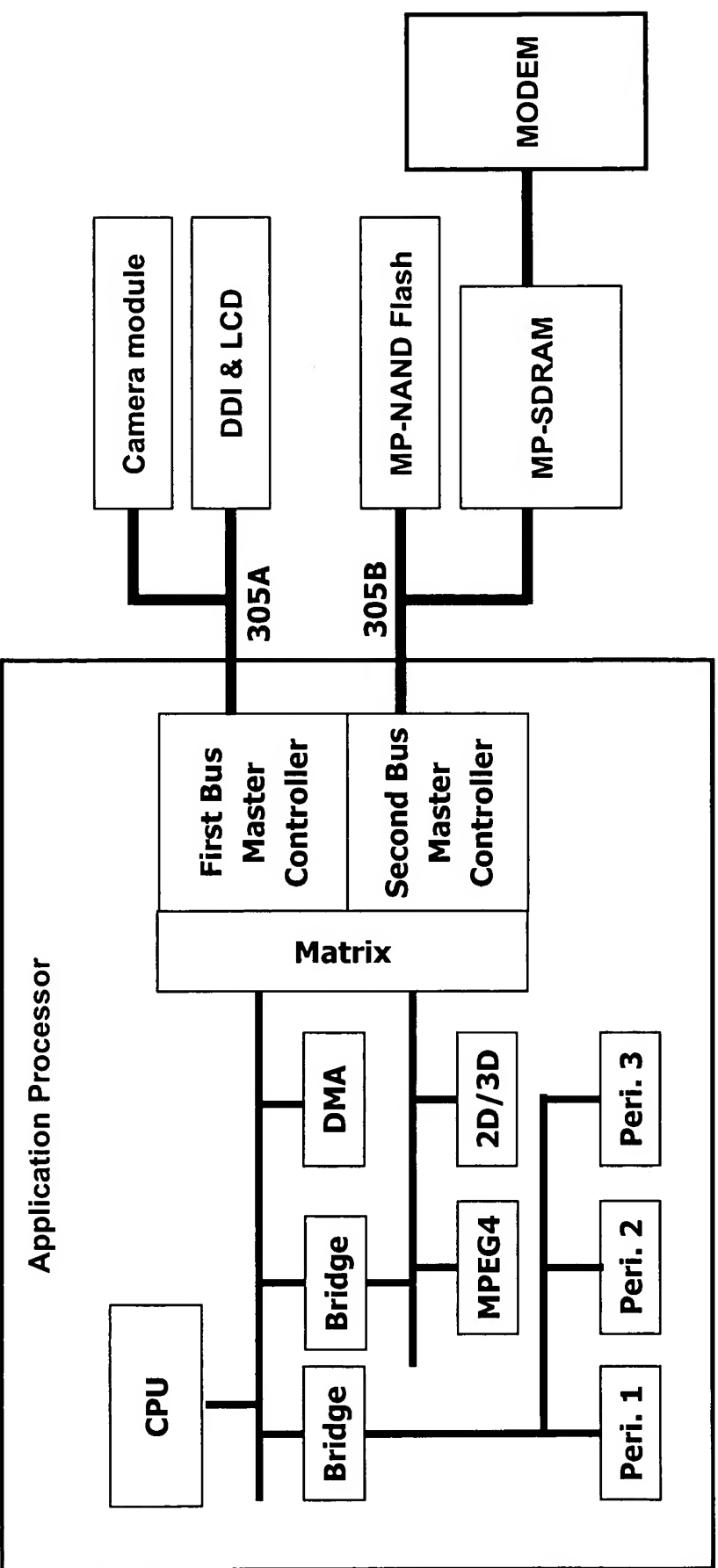


Fig.5

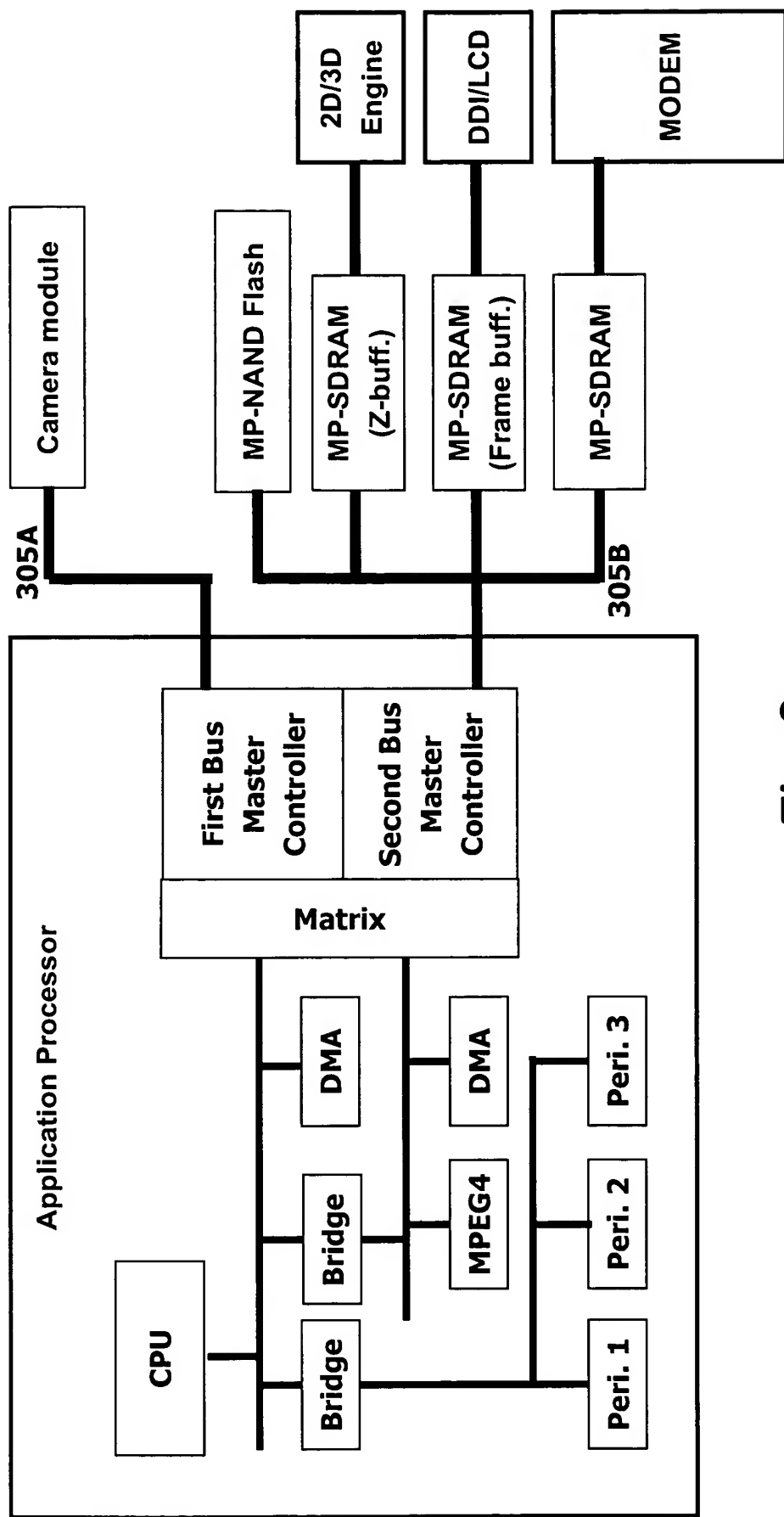


Fig.6

Name	Signal Description
nCS	Chip Select signal, active low
CnD	Command Packet (High) or Data Packet (Low)
nRW	Transfer direction of the Data Pins (DIO) Master Write (High) or Read (Low)
CLK	Forwarded Clock, CMD & write-data packets are synchronized on this clock
DIO[3:0]	4-bit bi-directional data bus
RESP	Returned Clock, read-data packets are synchronized on this clock
STAT	Response of the Slave device

Fig.7

	bit				
	3	2	1	0	
0	R	-	TY		
1	-	-	CL		
2	DL				
3	$A_0$				
$\sim$	$\sim$				
$i+2$	$A_i$				

Fig.8



Field Name	Width	Description
R	1	This field specifies the target of the current transaction. The master can access the internal registers of the slave device or the actual data which will be supplied by the slave device. 0 – Access normal data 1 – Access the internal register of the slave device
TY	2	This field specifies the type of the current transfer. 00 – Read Transfer 01 – Reserved 10 – Write Transfer 11 – Reserved
CL	2	This field specifies the length of the CMD Packet. 00 – 4 x 4-bit      01 – 8 x 4-bit 10 – 12 x 4-bit     11 – 16 x 4-bit
DL	4	This field specifies the size of the Data Packet. Data-Packet Size = $2^{\text{DL}}$ bytes (1, 2 ~ 32,768 bytes)
$A_0 \sim A_i$	$4 \times (i+1)$	These fields include the start address of the requested transfer

Fig.9

Address (byte)	Description
0	Manufacturer ID
1	
2	Version Number
3	Device Type
4	Max. Operational Frequency
5	
6	Master Command
7	Internal Buffer Control
8	Read Buffer Pending-Transaction Count
9	Write Buffer Pending-Transaction Count
A	Internal Buffer Size
B	
C	Write Buffer Base Address
D	
E	Reserved
F	Transaction Error

Fig.10

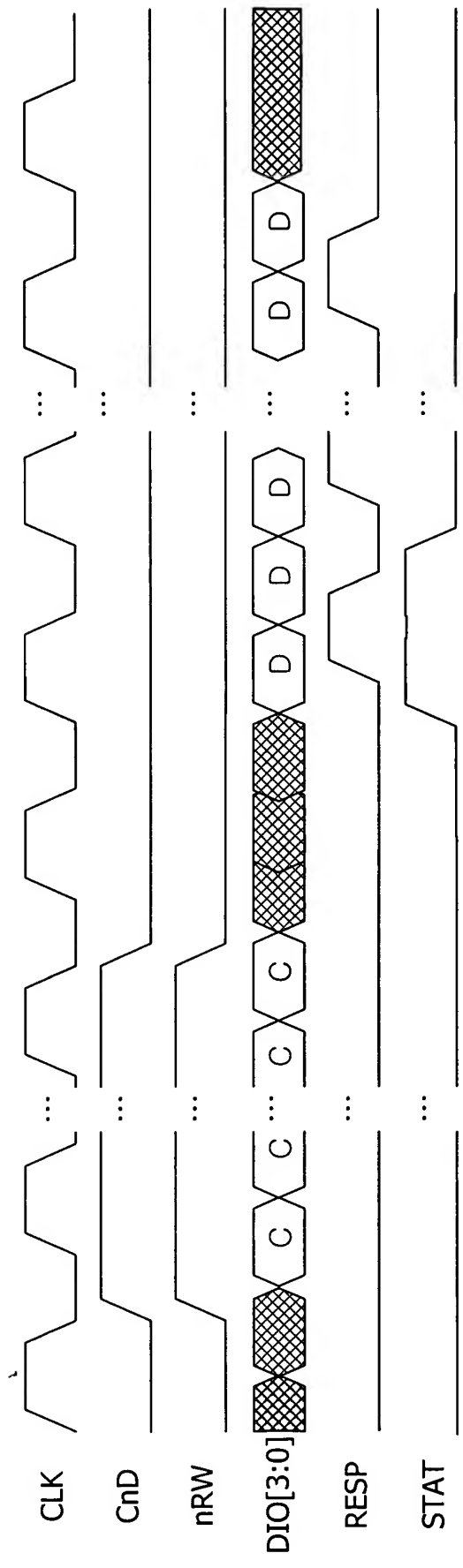


Fig.11

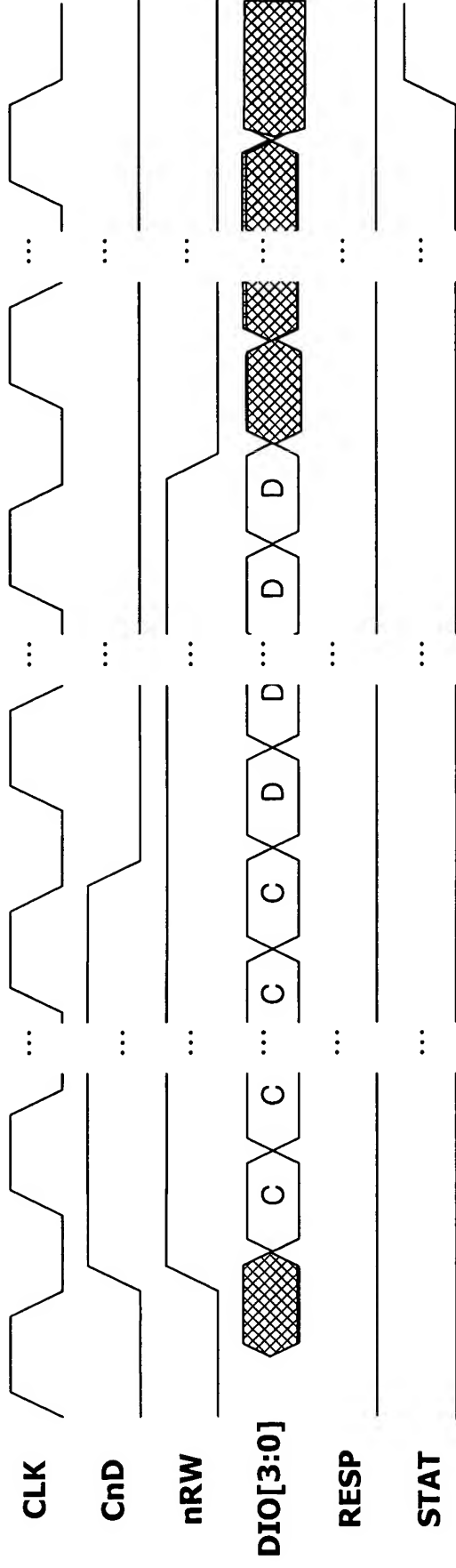


Fig.12

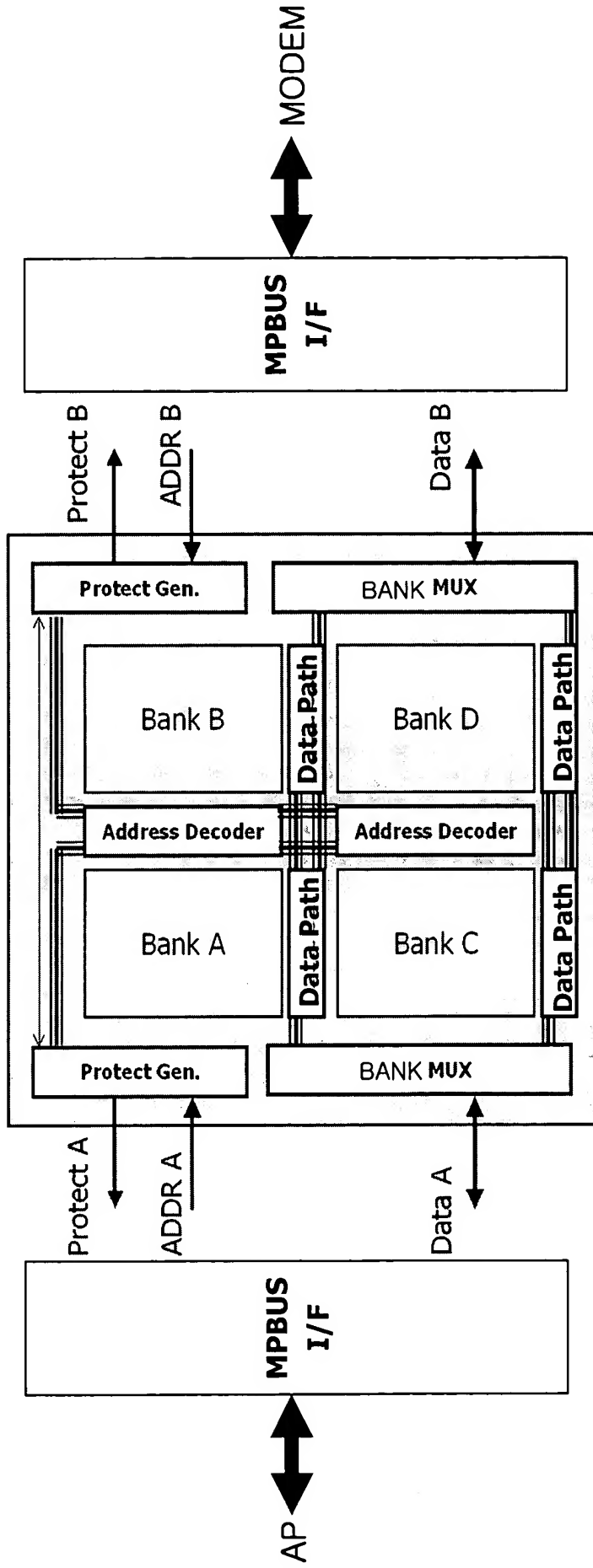


Fig. 13

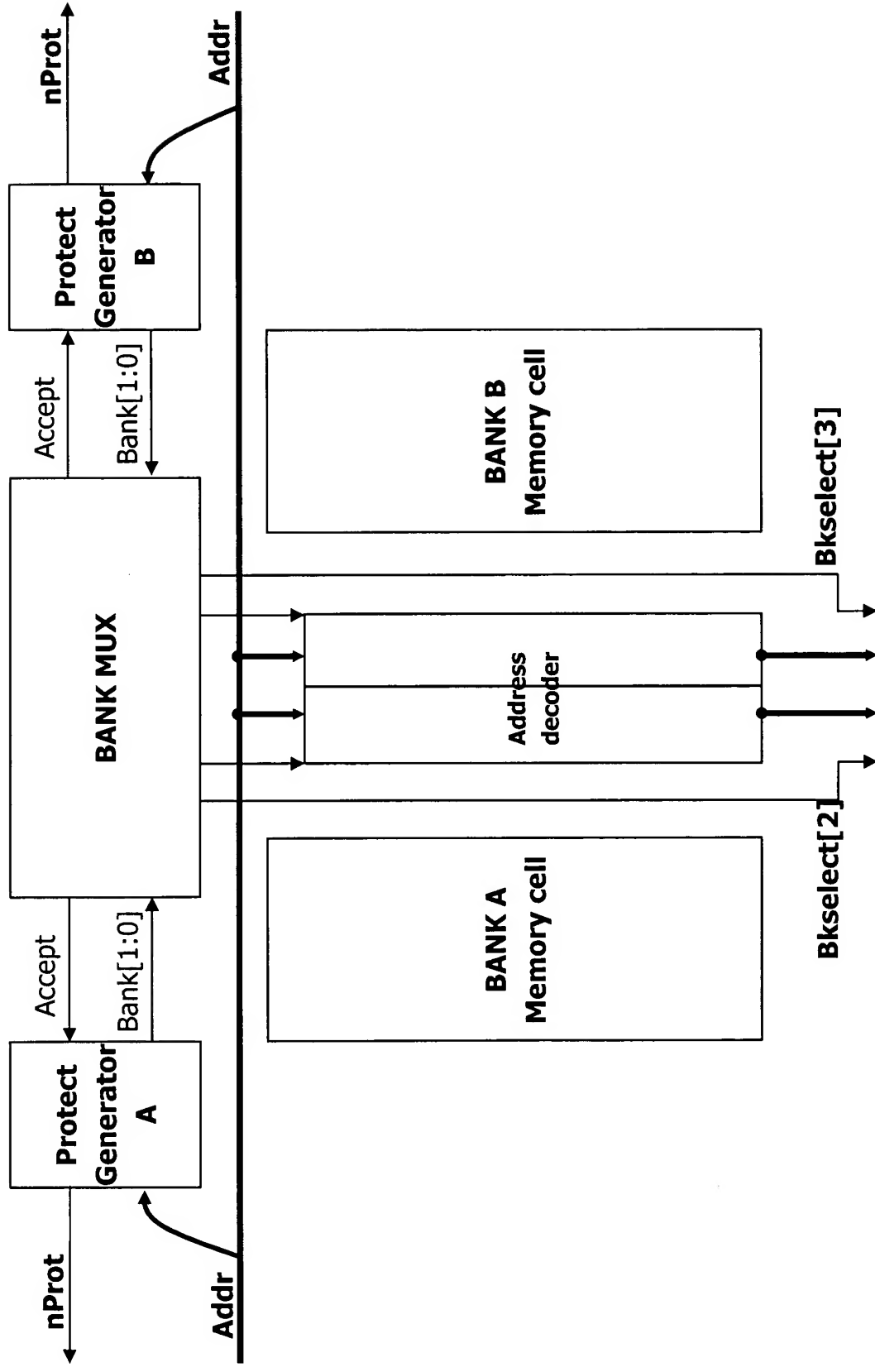


Fig.14

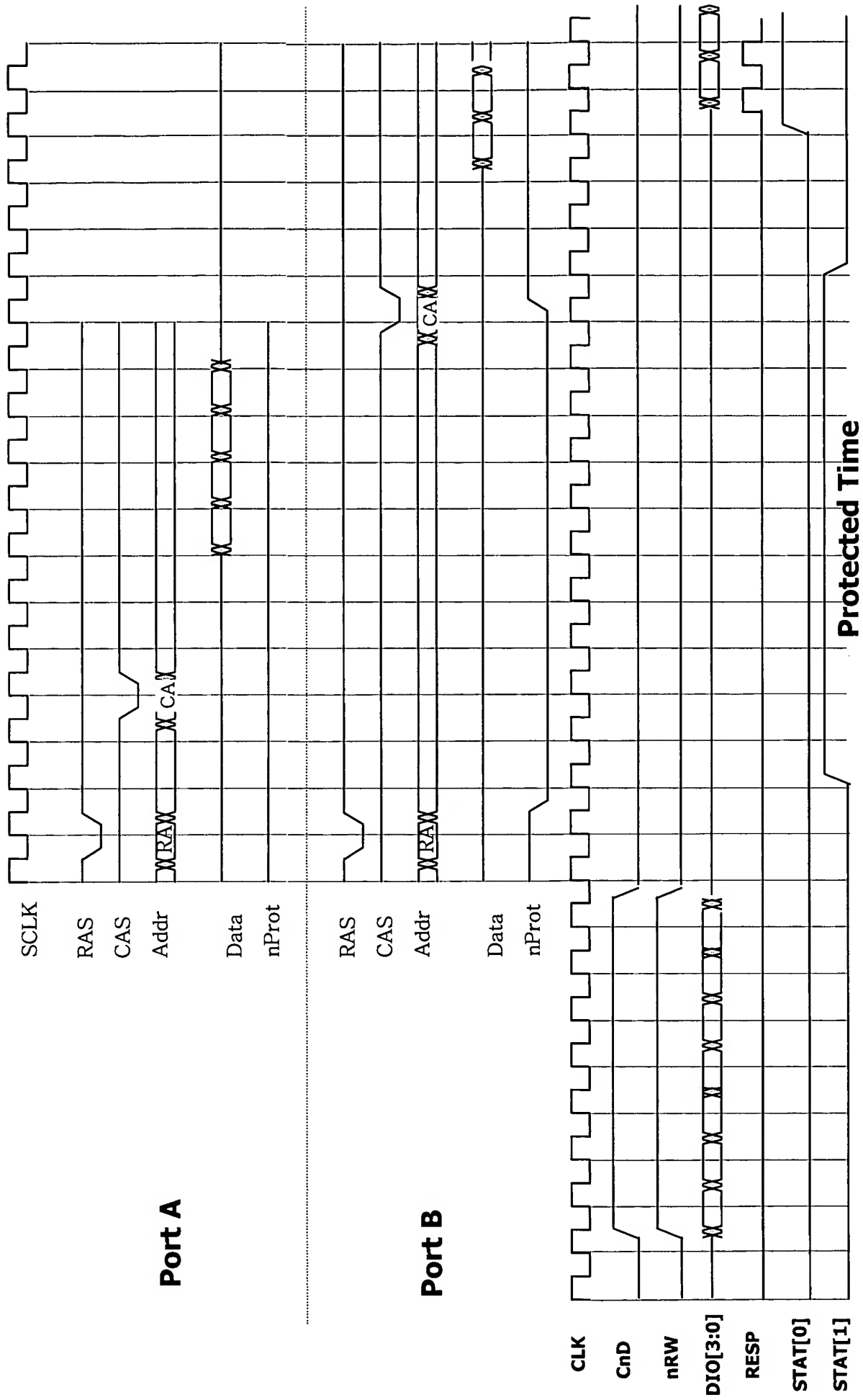


Fig. 15